

## Single N-Channel Enhancement Mode MOSFET

$V_{DS}=70V$ ,  $I_D=80A$ ,  $R_{DS(ON)}=5.9\ m\Omega$

### DESCRIPTION

The OR7080 is N-Channel logic enhancement mode power field effect transistors designed for high current switching applications.

Rugged  $E_{AS}$  capability and ultra low  $R_{DS(ON)}$  is suitable for PWM, load switching especially for E-Bike controller applications.

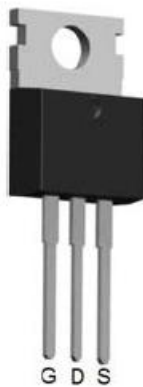
### FEATURE

- ◆  $70V/80A$ :  $R_{DS(ON)} < 7.2m\Omega @ V_{GS}=10V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Special designed for E-bike controller
- ◆ Full RoHS compliance
- ◆ TO-220, TO-263 package design

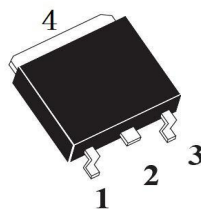
### APPLICATIONS

- ◆ 48V E-bike controller applications
- ◆ Hard switched and high frequency circuits
- ◆ Power supply

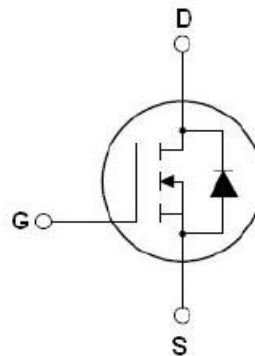
### PIN CONFIGURATION



To-220 Top View



TO-263



Schematic Diagram

## ■ ABSOLUTE MAXIMUM RATINGS ( $T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Symbol	Parameter	Typical	Unit
$V_{DSS}$	Drain-Source Voltage	70	V
$V_{GSS}$	Gate-Source Voltage	+25	V
$I_D$	Continuous Drain Current( $T_J=150^{\circ}\text{C}$ )	$V_{GS}=-10\text{V}$ 80	A
$I_{DM}$	Pulsed Drain Current	320	A
$T_J$	Operation Junction Temperature	-55~150	$^{\circ}\text{C}$
$T_{STG}$	Storage Temperature Range	-55~150	$^{\circ}\text{C}$
$P_D$	Power Dissipation( $T_C=25^{\circ}\text{C}$ )	100	W
$E_{AS}$	Single Pulse Avalanche Energy ( $T_J=25^{\circ}\text{C}, V_{DD}=40\text{V}, V_{GS}=10\text{V}, R_G=25\Omega$ )	410	mJ
$R_{\theta JC}$	Thermal Resistance-Junction to Ambient	1.25	$^{\circ}\text{C}/\text{W}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ ELECTRICAL CHARACTERISTICS ( $T_A=25^{\circ}\text{C}$ Unless otherwise noted)

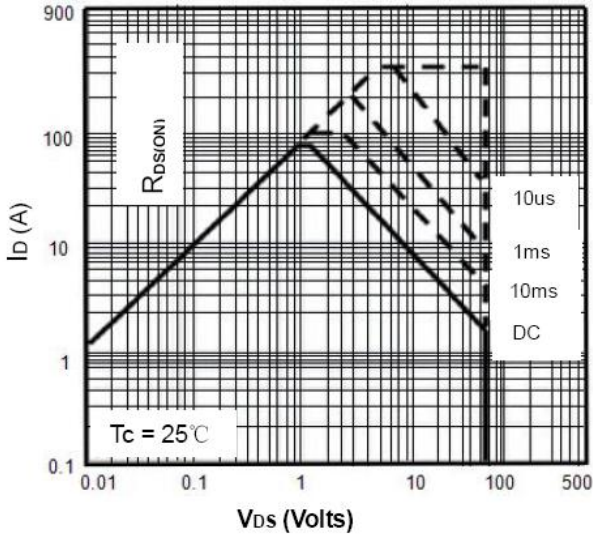
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_{DS}=250\mu\text{A}$	70	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{CS}, I_{DS}=250\mu\text{A}$	2	-	4	V
$I_{GSS}$	Gate Leakage Current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$	-	-	+100	nA
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=68\text{V}, V_{GS}=0\text{V}$ $T_C=25^{\circ}\text{C}$	-	-	1	$\mu\text{A}$
		$V_{DS}=68\text{V}, V_{GS}=0\text{V}$ $T_C=125^{\circ}\text{C}$	-	-	10	$\mu\text{A}$
$R_{DS(ON)}$	Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_{DS}=40\text{A}$	-	5.9	7.2	m $\Omega$
Source-Drain Diode						
$I_S$	Diode Forward Current (Max.)		-	92	-	A
$V_{SD}$	Diode Forward Voltage	$I_S=40\text{A}, V_{GS}=0\text{V}$		0.69	0.95	V
Dynamic Parameters						
$Q_g$	Total Gate Charge	$V_{DS}=50\text{V}, V_{GS}=10\text{V}$ $I_D=40\text{A}$	-	82	-	nC
$Q_{gs}$	Gate-Source Charge		-	16.2	-	
$Q_{gd}$	Gate-Drain Charge		-	36.7	-	
$C_{iss}$	Input Capacitance	$V_{DS}=25\text{V}, V_{GS}=0\text{V}$ $F=1\text{MHz}$	-	3483	-	pF
$C_{oss}$	Output Capacitance		-	459	-	
$C_{rss}$	Reverse Transfer Capacitance		-	214	-	
$t_{d(on)}$	Turn-On Time	$V_{DS}=30\text{V}, R_L=15\Omega$ $V_{GS}=10\text{V}, R_G=2.5\Omega$	-	11	-	nS
$t_r$			-	13	-	
$t_{d(off)}$	Turn-Off Time		-	22	-	
$t_f$			-	37	-	

Note: 1. Pulse test: pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ ;

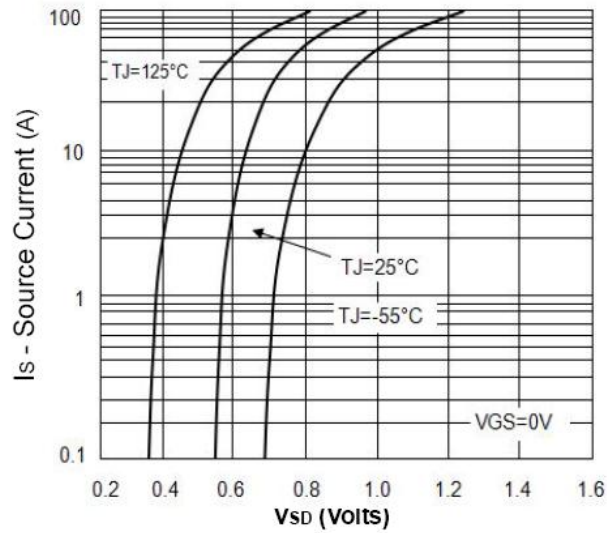
2. Static parameters are based on package level with recommended wire-bonding

**TYPICAL CHARACTERISTICS** ( $T_A=25^{\circ}C$  Unless otherwise noted)

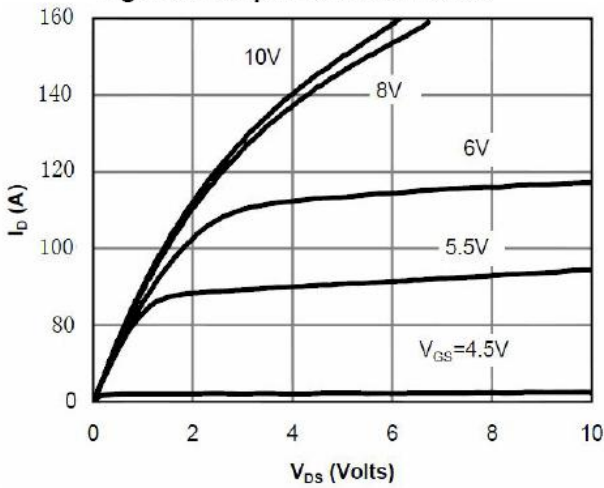
**Figure1. Safe Operating Area**



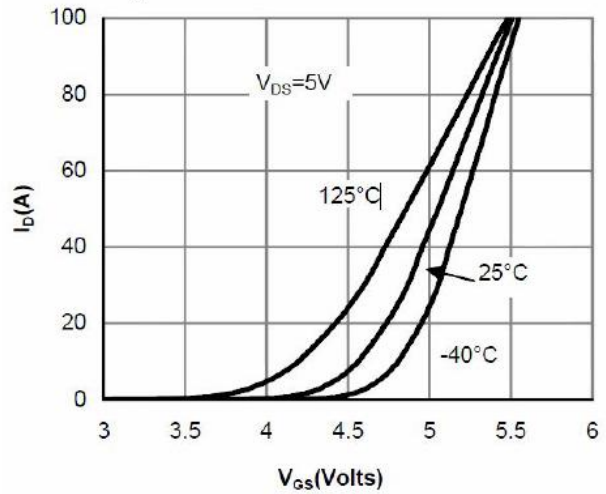
**Figure2. Source-Drain Diode Forward Voltage**



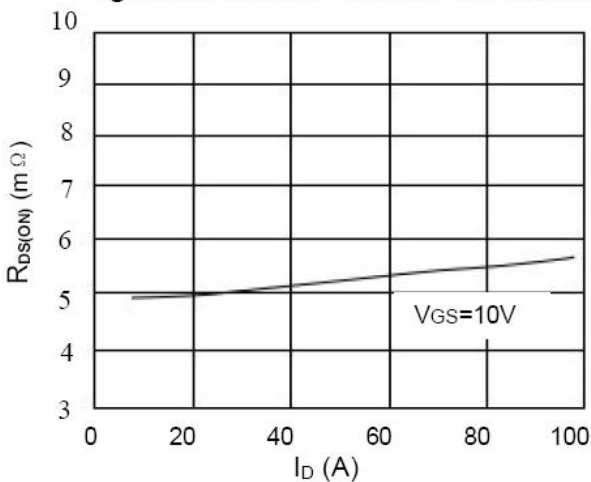
**Figure3. Output Characteristics**



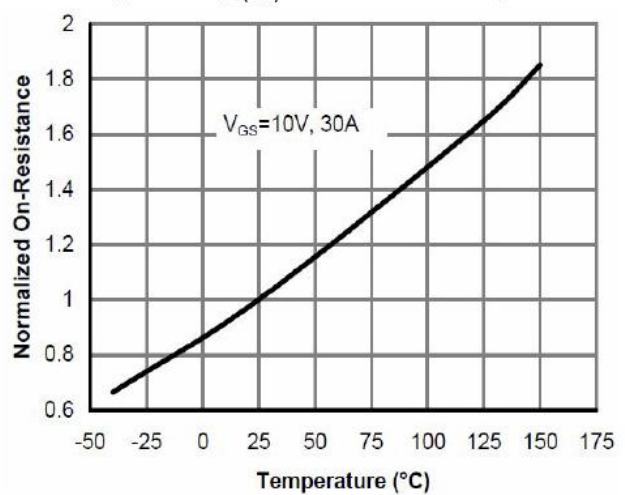
**Figure4. Transfer Characteristics**



**Figure5. Static Drain-Source On Resistance**

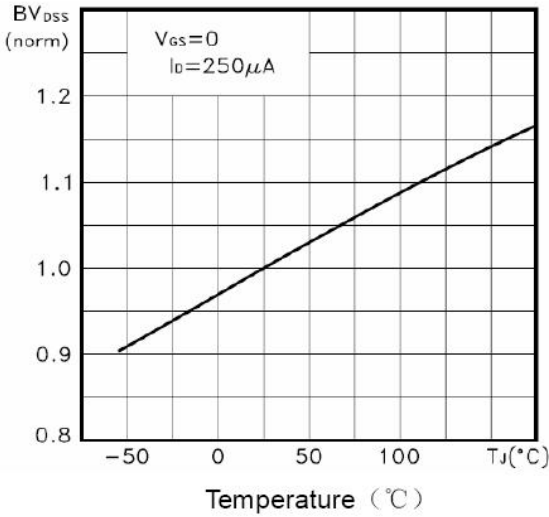


**Figure6.  $R_{DS(ON)}$  vs Junction Temperature**

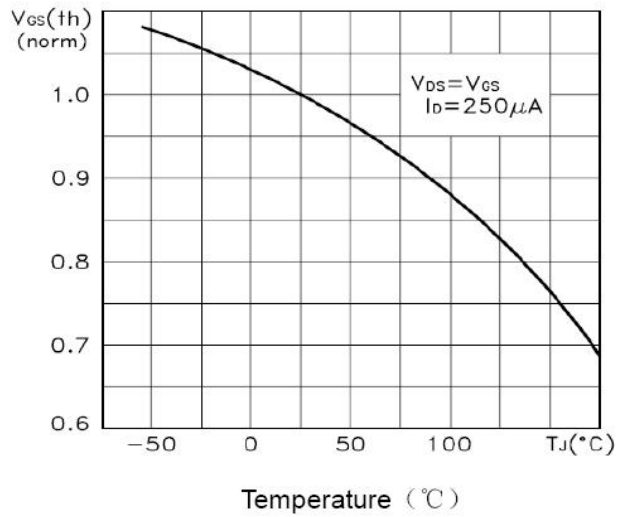


**TYPICAL CHARACTERISTICS** ( $T_A=25^{\circ}C$  Unless otherwise noted) (Continue)

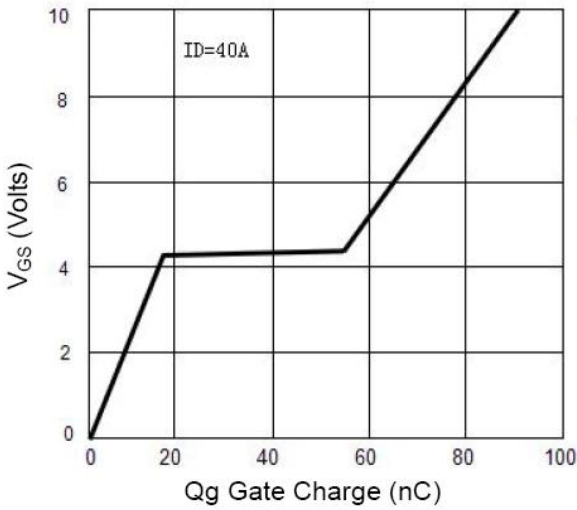
**Figure7.  $BV_{DSS}$  vs Junction Temperature**



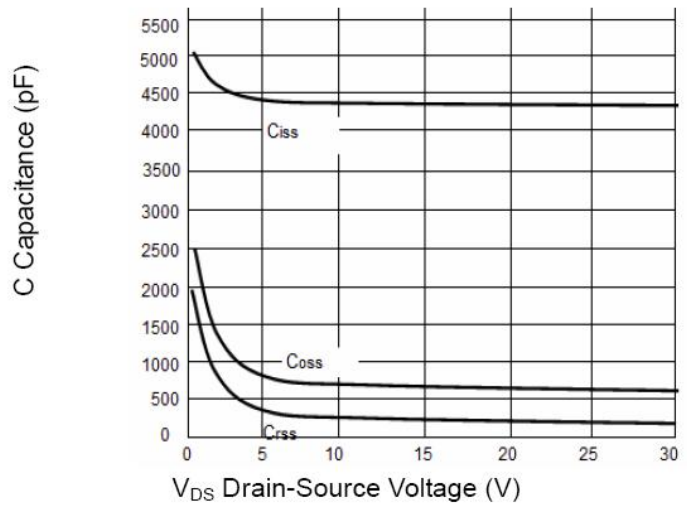
**Figure8.  $V_{GS(th)}$  vs Junction Temperature**



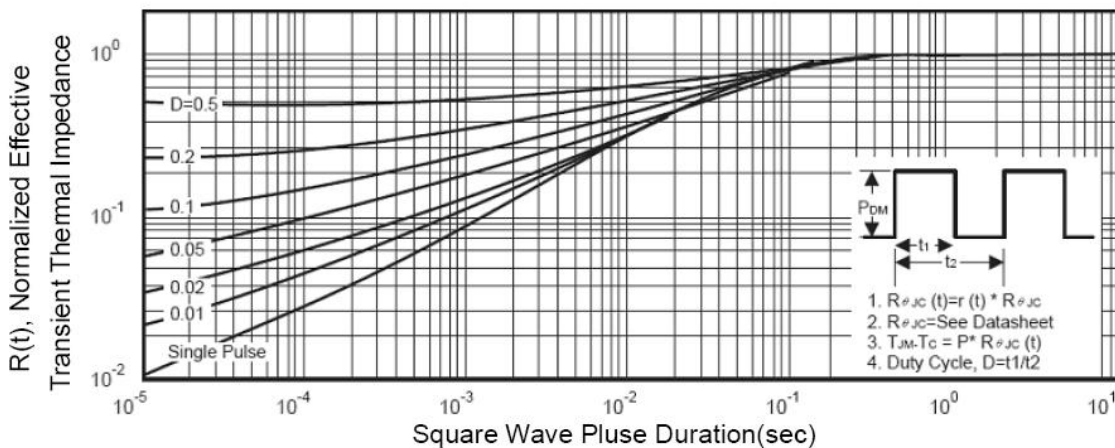
**Figure9. Gate Charge Waveforms**



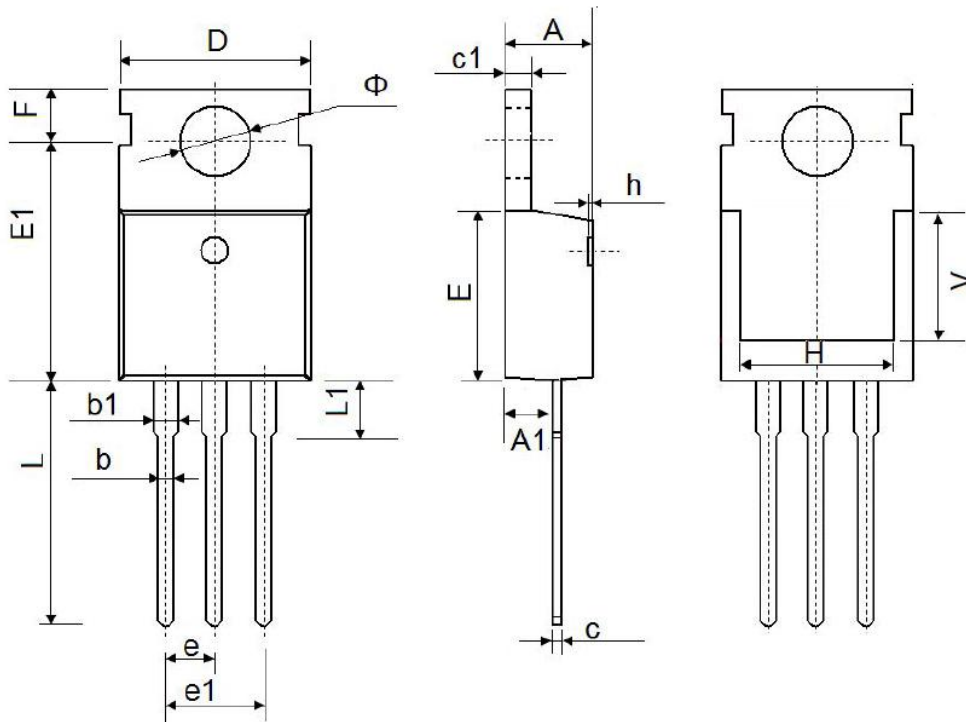
**Figure10. Capacitance**



**Figure11. Normalized Maximum Transient Thermal Impedance**



## T0-220 PACKAGE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150